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TITLE

A method of etching a mask layer and a protecting layer for metal contact windows

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates in general to an etching method, and particularly to a method of etching a mask layer and protecting layer for metal contacting window.

Description of the Related Art

With the technology of integrated circuits evolving, device sizes have reached sub-micron, half-micron, deep sub-micron and very deep sub-micron levels. Because of reduced device size, there can be more IC devices in one chip. It also means that chips have better performance. Therefore, etching technology plays a very important role. Desired circuit patterns being presented accurately depends on etching technology. High density plasma (HDP) etching technology has been widely applied in etching silicon dioxide layer, silicon nitride layer, polysilicon layer and metal layer.

The prior art utilizing high density plasma to etch a thin film is shown in FIG 1A-1C. In FIG. 1A, a silicon oxide layer

12 and a thin film, such as polysilicon layer 14, are formed on a silicon substrate 10 in sequence. The thin film is designed in a pattern on the surface for the following etching. Then, a photoresist layer 16 is coated on the polysilicon 14 and defines the pattern through photolithography, as shown in FIG. 1B. The polysilicon 14 undergoes high density plasma etching to form a pattern 18 using the photoresist layer with the defined patterns, as shown in FIG. 1C. After etching, the developed photoresist 16 is removed. High density plasma etching is dry etching. Vertical side-walls are obtained by this technology because a protecting film (not shown) is formed on the side-walls of polysilicon during dry etching, such that the etching is anisotropic. Forming the protecting film depends strongly on the reaction gases, the etched material and the photoresist. If any of the factors is incomplete, the etching is isotropic.

However, in order to obtain patterns with higher resolution, a thin photoresist layer is required. Etching selectivity between a thin photoresist layer and an etched material is not good enough, however, with the result that the surface of the etched photoresist is not flat, as shown in FIG. 1C. Therefore, hard mask use in etching has been developed, as shown in FIG. 2A-2E. In FIG. 2A, a silicon dioxide layer 21 and a polysilicon layer 22 are formed on a silicon substrate 20 in sequence. In 2B, a silicon dioxide layer 23 (or a silicon nitride) is formed

on the polysilicon 22. A photoresist layer 24 is spin-coated over the silicon dioxide layer 23. After coating, photolithography is performed and the resulting structure is shown in FIG. 2C. Then, the silicon dioxide layer 23 is etched to form a hard mask 25 using the pattern defined photoresist 24 to be the mask. The photoresist 24 is removed, as shown in FIG. 2D. Finally, high density plasma etching is performed on the polysilicon layer 22 to form patterns 26 using the hard mask 25. However, because the protecting film cannot be formed, this etching results in an undercutting, as shown in FIG. 2E. The desired circuit can't be presented exactly.

SUMMARY OF THE INVENTION

The object of the present invention is a method of etching a mask layer to act as a protecting layer for metal contact windows using a victim layer with slopes to avoid undercutting.

According to the present invention, a method for solving the undercutting on the sidewalls of the etched layer includes the following steps. First, a mask layer is formed on a semiconductor substrate. Next, a photoresist with patterns is formed on the surface of the mask layer. Next, a victim layer is formed on the surface of the photoresist according to the photoresist topography, wherein the thickness of the victim layer is less than that of the photoresist, such that a plurality

of slopes are formed on the sidewalls of the photoresist. Then, the photoresist and the victim layer with slopes are used as the etching mask for etching the mask layer to form patterns.

With the above flow, the desired circuit patterns can be presented accurately after solving the undercutting.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given herein below and the accompanying drawings, given by way of illustration only and thus not intended to be limitative of the present invention.

FIGs. 1A-1C are sectional diagrams showing high density etching according to the prior art.

FIGs. 2A-2E are sectional diagrams showing an etching using a hard mask according to the prior art.

FIGs. 3A-3D are sectional diagrams showing an etching of a preferred embodiment according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In FIG. 3, a silicon substrate 30 is provided. A semiconductor device and inner leads are formed on the silicon substrate 30 (not shown). A protecting layer 31, such as nitride, is formed on the inner leads by the prior art of depositing thin film technology to protect from moisture, metal

ions attacking and mechanical scrape. The prior art of depositing thin film technology is chemical vapor deposition (CVD), such as plasma enhanced CVD, low pressure CVD or atmospheric CVD. After forming a protecting layer 31, a photoresist layer 32 is spin-coated on the protecting layer 31.

In FIG. 3B, patterns 33 are defined and formed on the photoresist layer 32 through photolithography. Next, a victim layer 34 is formed on the surface of the patterns 33 according to the pattern topography, as shown in FIG. 3C. The victim layer 34 material is an anti-reflection coating. Additionally, the thickness of the victim layer 34, less than the photoresist 33, is about 800~1000Å. The optimum thickness is 900Å. The contour of the victim layer 34 contains slopes 34a on photoresist sidewalls 33a.

Then, etching is performed on the protecting layer 31, and both the photoresist 32 and the victim layer 34 are used as the mask. As a result, pad regions 35 and fuse regions 36 are defined and formed a plurality of metal contacting windows. According to the present invention, there is no undercut on the sidewalls 31a of the protecting layer after etching, as shown in FIG. 3D. The circuit patterns are defined and developed precisely.

The foregoing description of the preferred embodiments of this invention has been presented for purposes of illustration and description. Obvious modifications or variations are

possible in light of the above teaching. The embodiments were chosen and described to provide the best illustration of the principles of this invention and its practical application to thereby enable those skilled in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the present invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally, and equitably entitled.